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1 Timestamp snooping: an approach for extending SMPs

Milo M. K. Martin, Daniel J. Sorin, Anastassia Ailamaki, Alaa R. Alameldeen, Ross M. Dickson, Carl J. Mauer, Kevin E. Moore, Manoj Plakal, Mark D. Hill, David H. Wood
November 2000 **ACM SIGPLAN Notices**, Volume 35 Issue 11
Publisher: ACM

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Symmetric multiprocessor (SMP) servers provide superior performance for the commercial workloads that dominate the Internet. Our simulation results show that over one-third of cache misses by these applications result in cache-to-cache transfers, where ...

2 Timestamp snooping: an approach for extending SMPs

Milo M. K. Martin, Daniel J. Sorin, Anatassia Ailamaki, Alaa R. Alameldeen, Ross M. Dickson, Carl J. Mauer, Kevin E. Moore, Manoj Plakal, Mark D. Hill, David A. Wood
November 2000 **ASPLOS-IX:** Proceedings of the ninth international conference on Architectural support for programming languages and operating systems
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Symmetric muultiprocessor (SMP) servers provide superior performance for the commercial workloads that dominate the Internet. Our simulation results show that over one-third of cache misses by these applications result in cache-to-cache transfers, where ...

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December 2000 **ASPLOS-IX: ACM SIGOPS Operating Systems Review,**
Volume 34 Issue 5
Publisher: ACM

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Symmetric muultiprocessor (SMP) servers provide superior performance for the commercial workloads that dominate the Internet. Our simulation results show that over one-third of cache misses by these applications result in cache-to-cache transfers, where ...

4 Tuning data replication for improving behavior of MPSoC applications
O. Ozturk, M. Kandemir, M. J. Irwin, I. Kolcu
April 2004 **GLSVLSI '04:** Proceedings of the 14th ACM Great Lakes symposium on VLSI
Publisher: ACM

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Maintaining cache coherence can be very costly for on-chip multiprocessors from an energy perspective. Observing this, we propose a compiler-directed strategy that replicates array data in cache memories of its potential consumer processors at the time ...

Keywords: MPSoC, cache coherence, data replication, optimizing compiler, power consumption

5 Timestamp snooping: an approach for extending SMPs
Milo M. K. Martin, Daniel J. Sorin, Anatassia Ailamaki, Alaa R. Alameldeen, Ross M. Dickson, Carl J. Mauer, Kevin E. Moore, Manoj Plakal, Mark D. Hill, David A. Wood
December 2000 **ASPLOS-IX: ACM SIGARCH Computer Architecture News,** Volume 28 Issue 5
Publisher: ACM

Full text available: pdf(164.27 KB)
Additional Information: full citation, abstract, references, cited by, index terms

Symmetric muultiprocessor (SMP) servers provide superior performance for the commercial workloads that dominate the Internet. Our simulation results show that over one-third of cache misses by these applications result in cache-to-cache transfers, where ...

6 Efficient data protection for distributed shared memory multiprocessors
Brian Rogers, Milos Prvulovic, Yan Solihin
September 2006 **PACT '06:** Proceedings of the 15th international conference on Parallel architectures and compilation techniques
Publisher: ACM

Full text available: pdf(386.29 KB)
Additional Information: full citation, abstract, references, index terms

Data security in computer systems has recently become an increasing concern, and hardware-based attacks have emerged. As a result, researchers have investigated hardware encryption and authentication mechanisms as a means of addressing this security ...

Keywords: DSM multiprocessor, data security, memory encryption and authentication

7 Overlapping dependent loads with addressless preload

Zhen Yang, Xudong Shi, Feiqi Su, Jih-Kwon Peir

September 2006 **PACT '06:** Proceedings of the 15th international conference on Parallel architectures and compilation techniques

Publisher: ACM

Full text available: pdf(245.53 KB)   Additional Information: full citation, abstract, references, index terms

Modern out-of-order processors with non-blocking caches exploit Memory-Level Parallelism (MLP) by overlapping cache misses in a wide instruction window. The exploitation of MLP, however, can be limited due to long-latency operations in producing the ...

Keywords: data prefetching, instruction and issue window, memory-level parallelism, pointer-chasing loads

8 Fast and fair: data-stream quality of service

Thomas Y. Yeh, Glenn Reinman

September 2005 **CASES '05:** Proceedings of the 2005 international conference on Compilers, architectures and synthesis for embedded systems

Publisher: ACM

Full text available: pdf(318.10 KB)   Additional Information: full citation, abstract, references, cited by, index terms

Chip multiprocessors have the potential to exploit thread level parallelism, particularly in the context of embedded server farms where the available number of threads can be quite high. Unfortunately, both per-core and overall throughput are significantly ...

Keywords: CMP, NUCA, PDAS, QOS, adaptive, bandwidth, cache, chip multiprocessor, cluster, data-stream, distributed, embedded, memory wall, migration, non-uniform access, partition, per thread degradation, phase

9 *L-diversity: Privacy beyond k-anonymity*

Ashwin Machanavajjhala, Daniel Kifer, Johannes Gehrke, Muthuramakrishnan Venkitasubramaniam

March 2007 **ACM Transactions on Knowledge Discovery from Data (TKDD)**, Volume 1 Issue 1

Publisher: ACM

Full text available: pdf(838.00 KB)   Additional Information: full citation, abstract, references, index terms

Publishing data about individuals without revealing sensitive information

about them is an important problem. In recent years, a new definition of privacy called *k*-anonymity has gained popularity. In a *k*-anonymized dataset, each record ...

Keywords: ℓ-diversity, *k*-anonymity, Data privacy, privacy-preserving data publishing

10 Quantifying eavesdropping vulnerability in sensor networks
Madhukar Anand, Zachary Ives, Insup Lee
August 2005 **DMSN '05:** Proceedings of the 2nd international workshop on
             Data management for sensor networks
Publisher: ACM

Additional Information: full citation, abstract,
Full text available: pdf(514.26 KB)   references, cited by, index
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With respect to security, sensor networks have a number of considerations that separate them from traditional distributed systems. First, sensor devices are typically vulnerable to physical compromise. Second, they have significant power and processing ...

Keywords: data streams, eavesdropping, probability distribution, wireless sensor networks

11 REED: robust, efficient filtering and event detection in sensor
networks
Daniel J. Abadi, Samuel Madden, Wolfgang Lindner
August 2005 **VLDB '05:** Proceedings of the 31st international conference on
             Very large data bases
Publisher: VLDB Endowment

Additional Information: full citation, abstract,
Full text available: pdf(286.61 KB)   references, cited by, index
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This paper presents a set of algorithms for efficiently evaluating join queries over static data tables in sensor networks. We describe and evaluate three algorithms that take advantage of distributed join techniques. Our algorithms are capable of running ...

12 A regulated transitive reduction (RTR) for longer memory race
recording
Min Xu, Mark D. Hill, Rastislav Bodik
November 2006 **ASPLOS-XII: ACM SIGPLAN Notices**,   Volume 41 Issue 11
Publisher: ACM

Full text available: pdf(524.02 KB) Additional Information: full citation, abstract,
                                      references, index terms

Now at VMware. Multithreaded deterministic replay has important applications in cyclic debugging, fault tolerance and intrusion analysis. Memory race recording is a key technology for multithreaded deterministic replay. In this paper, we considerably ...

Keywords: determinism, multithreading, race recording

13 Flush: a reliable bulk transport protocol for multihop wireless networks

Sukun Kim, Rodrigo Fonseca, Prabal Dutta, Arsalan Tavakoli, David Culler, Philip Levis, Scott Shenker, Ion Stoica

November 2007 **SenSys '07:** Proceedings of the 5th international conference on Embedded networked sensor systems

Publisher: ACM

Full text available: pdf(421.18 KB) Additional Information: full citation, abstract, references, index terms

We present Flush, a reliable, high goodput bulk data transport protocol for wireless sensor networks. Flush provides end-to-end reliability, reduces transfer time, and adapts to time-varying network conditions. It achieves these properties using end-to-end ...

Keywords: interference, transport, wireless sensor networks

14 Toward a threat model for storage systems

Ragib Hasan, Suvda Myagmar, Adam J. Lee, William Yurcik

November 2005 **StorageSS '05:** Proceedings of the 2005 ACM workshop on Storage security and survivability

Publisher: ACM

Additional Information: full citation, abstract, references, cited by, index terms

Full text available: pdf(258.24 KB)

The growing number of storage security breaches as well as the need to adhere to government regulations is driving the need for greater storage protection. However, there is the lack of a comprehensive process to designing storage protection solutions. ...

Keywords: security, storage system, threat model

15 Greening of the internet

Maruti Gupta, Suresh Singh

August 2003 **SIGCOMM '03:** Proceedings of the 2003 conference on Applications, technologies, architectures, and protocols for computer communications

Publisher: ACM

Additional Information: full citation, abstract, references, cited by, index terms

Full text available: pdf(175.00 KB)

In this paper we examine the somewhat controversial subject of energy consumption of networking devices in the Internet, motivated by data collected by the U.S. Department of Commerce. We discuss the impact on network protocols of saving energy by putting ...

Keywords: energy, internet, protocols

16 Building Intrusion-Tolerant Secure Software

Tao Zhang, Xiaotong Zhuang, Santosh Pande

March 2005 **CGO '05:** Proceedings of the international symposium on Code
                generation and optimization
Publisher: IEEE Computer Society

Full text available: pdf(234.98 KB)   Additional Information: full citation, abstract, index
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In this work, we develop a secret sharing based compiler solution to
achieve confidentiality, integrity and availability (intrusion tolerance) of
critical data together, rather than tackling them one by one as in
previous approaches. Under our scheme, ...

17 Multiplex: unifying conventional and speculative thread-level
parallelism on a chip multiprocessor
Chong-Liang Ooi, Seon Wook Kim, Il Park, Rudolf Eigenmann, Babak
Falsafi, T. N. Vijaykumar
June 2001 **ICS '01:** Proceedings of the 15th international conference on
                Supercomputing
Publisher: ACM

                                        Additional Information: full citation, abstract,
Full text available: pdf(155.15 KB)   references, cited by, index
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Recent proposals for Chip Multiprocessors (CMPs) advocate speculative,
or implicit, threading in which the hardware employs prediction to peel
off instruction sequences (i.e., implicit threads) from the sequential
execution stream and speculatively executes ...

18 Optimizing Replication, Communication, and Capacity Allocation in
CMPs
Zeshan Chishti, Michael D. Powell, T. N. Vijaykumar
June 2005 **ISCA '05:** Proceedings of the 32nd annual international
                symposium on Computer Architecture
Publisher: IEEE Computer Society

Full text available: pdf(166.45 KB)   Additional Information: full citation, abstract, cited by,
                                                                                index terms

Chip multiprocessors (CMPs) substantially increase capacity pressure on
the on-chip memory hierarchy while requiring fast access. Neither
private nor shared caches can provide both large capacity and fast
access in CMPs. We observe that compared to symmetric ...

19 Verification techniques for cache coherence protocols
Fong Pong, Michel Dubois
March 1997 **ACM Computing Surveys (CSUR),**   Volume 29 Issue 1
Publisher: ACM

Full text available: pdf(1.25 MB)   Additional Information: full citation, abstract, references,
                                                                                cited by, index terms

In this article we present a comprehensive survey of various approaches
for the verification of cache coherence protocols based on state
enumeration, (symbolic model checking, and symbolic state models.

Since these techniques ...

Keywords: cache coherence, finite state machine, protocol verification, shared-memory multiprocessors, state representation and expansion

20 HIDE: an infrastructure for efficiently protecting information leakage on the address bus
Xiaotong Zhuang, Tao Zhang, Santosh Pande
December 2004 **ASPLOS-XI: ACM SIGARCH Computer Architecture News**, Volume 32 Issue 5
Publisher: ACM

Additional Information: full citation, abstract, references, cited by, index terms
Full text available: pdf(216.31 KB)

XOM-based secure processor has recently been introduced as a mechanism to provide copy and tamper resistant execution. XOM provides support for encryption/decryption and integrity checking. However, neither XOM nor any other current approach adequately ...

Keywords: address bus leakage protection, secure processor

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